# Optimized placement of microwave absorbers on high speed digital channels with SI, EMI and RFI considerations

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# Optimized placement of microwave absorbers on high speed digital channels with SI, EMI and RFI considerations

Todd Steigerwald, Advanced Micro Devices Inc.,

Mohammad Ali Khorrami, Laird Technologies,

Haris Chowdhry, Advanced Micro Devices Inc.,

Paul Dixon, Laird Technologies,

## Abstract

In this paper, the placement of microwave absorbers on the outer layers of multi-layer printed circuits boards (PCBs) with several high speed channels, to mitigate electromagnetic radiations from noisy transmission lines is investigated. New techniques to decrease the electromagnetic emissions from noisy digital circuitries are essential specifically in mobile devices that incorporate sensitive wireless radio receivers and noisy data buses in the proximity. Here, empirical results are presented to characterize the reduction of electromagnetic radiations from the PCB as the absorbers are applied while considering undesired consequences leading to the eye closure of the high speed channel. It is shown that the absorbers can introduce discontinuities along the transmission lines with high data rate signals which may lead to undesired reflections and transmission losses. Additionally, it can change the frequency-phase characteristics of the signal which might cause additional timing errors. Different optimized locations and types of the absorbers are studied to minimize the unwanted signal integrity consequences while reducing the electromagnetic radiation in targeted areas of the PCB. This analysis is mainly focused on a commercial second generation Peripheral Component Interconnect (PCIe) design. It is shown that the innovative usages and positioning of microwave absorbers can be useful in controlling electromagnetic interference while still keeping the signal integrity performance of the system minimally affected.

## Authors Biography

Todd W. Steigerwald has been involved in EMC Compliance Design techniques for over 20 years, and currently is a Senior EMC Engineer at Advanced Micro Devices working on CPU and APU processor silicon and platform design for EMI, RFI/wireless integration. Todd graduated from Texas A&M University with BS EET minoring in Physics, and currently holds 20 US Patents.

Mohammad Ali Khorrami received M.S. and PhD in Electrical Engineering from Tehran Poly-Technique University, and University of Arkansas in 2008 and 2014, respectively. He is currently working as a Scientist in Laird Technology Corporation. His major interests are signal and power integrity of high speed digital circuits, and Electromagnetic Compatibility.

Haris has over four years of experience in Signal Integrity and EMC simulation & validation. He is currently working at AMD as a Senior EMC engineer focusing on discrete graphics. He holds a Bachelor's Degree in Electrical Engineering from the University of Toronto and Master's Degree in Electrical Engineering from the University of Ontario.

Paul Dixon is a Staff Scientist at Laird specializing in electromagnetic modeling and characterization. Previously he was Director of Technology at Emerson & Cuming Microwave Products overseeing design and testing of advanced absorber solutions. He has a BS degree in Astrophysics from Michigan State and an MS in Microwave Engineering from the University of Massachusetts-Amherst.

## Introduction and background:

Nowadays, many mixed signal systems with digital processors and peripherals, and radiofrequency (e.g., Bluetooth, Wi-Fi, GPS, cellular data) transceivers are found in mobile devices and even inside desktops [1]. It is common that these systems have to be located in a close proximity to satisfy the stringent form factor requirements of mobile devices [2]. It is known that the digital circuits generate a very broadband radiated noise that may coincide with commonly used wireless communication bands. If the radiated noise levels are not taken into account in the mixed signal system design process, RF receivers (with sensitivities as low as -110 dBm) might easily be desensitized [3]. The RFI performance is evaluated and measured directly from a system's internal wireless antennas, sometimes only centimeters from PCB noise sources; and not measured in the far-field several meters from the system, as is required for EMC compliance measurements. These measurements are typically performed in dBm units, with specific RBW resolution bandwidths related to the specific communication link technology. Table 1 shows common RFI limits in a wireless embedded system. Considering the very low specified sensitivity level, it is important to maintain the isolation between different sections of the systems. However, this is becoming more challenging especially with the advent of upcoming generations of integrated circuits (ICs) that promise even higher clocking speeds and shorter signal rise and fall times. The likelihood of self-jamming (also called Radio Frequency Interference RFI) increases with the number of coexistent wireless devices, and as the size of the outer layer microstrip conductors become comparable to the wavelengths used by the radio receivers [4].

Table 1: Common wireless communication link specifications.

| BANDS (MHz) | Radio Standard | Measure RBW | Freq Range Start | Freq Range Stop | Specification |
|---|---|---|---|---|---|
| LTE Band 13 | LTE | 10 MHz | 746 MHz | 756 MHz | -95 dBm |
| 850 | GSM, CDMA, EV-DO, WCDMA | 200 kHz | 869 MHz | 894 MHz | -108 dBm |
| 900 | GSM | 200 kHz | 925 MHz | 960 MHz | -108 dBm |
| 1.575 GHz | GPS / GLONASS | 100 kHz | 1540 MHz | 1620 MHz | -114 dBm |
| 1800 | GSM | 200 kHz | 1805 MHz | 1880 MHz | -108 dBm |
| 1900 | GSM, CDMA, EV-DO, WCDMA | 200 kHz | 1930 MHz | 1990 MHz | -108 dBm |
| 2100 | WCDMA | 5 MHz | 2110 MHz | 2170 MHz | -97 dBm |
| 2400 | WLAN 2.4G | 100 kHz | 2400 MHz | 2480 MHz | -115 dBm |
| LTE High Band | LTE | 10 MHz | 2300 MHz | 2650 MHz | -95 dBm |
| 5100 | WLAN 5G | 100 kHz | 5100 MHz | 5800 MHz | -115 dBm |

In Fig. 1, several coupling paths between the digital and analog partitions are presented. The interference can be manifested by interaction between multiple sources and paths to the radio receiver. These include emissions from heatsinks, Switch Mode Power Supplies SMPS, switching noise propagating between power planes, and noise from high speed clock or bus traces routed on outer Microstrip layers. An appropriately designed mixed signal system is able to balance the requirements of interference sources, antenna

locations and other coupling paths to avoid receiver desensitization. However, there are cases that engineers need a fast and wideband solution to pass desired EMI regulatory limits, measured in the far-field; or to pass very stringent RFI internal limits while maintaining the signal integrity limitations of the digital circuitries. In these cases, the application of microwave absorbers might be a reliable solution to meet required emission goals by dissipating the extra electromagnetic energy into heat.

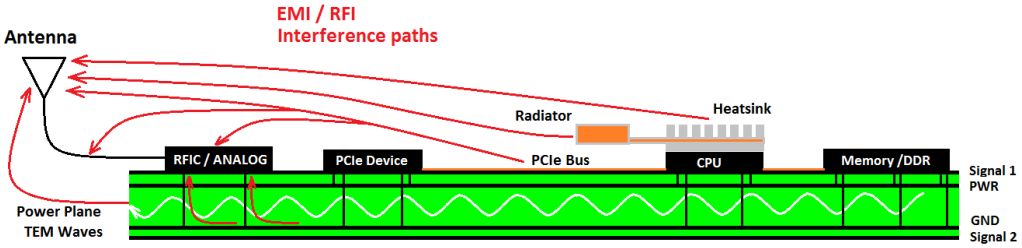



Fig. 1: A representation of inter-system interferences in a digital and RF system.

Here, the application of two different types of microwave absorbers over a second generation of Peripheral Component Interconnect express (PCIe Gen II) video channel is tested. In order to examine the influence of the absorbers on the radiated electromagnetic fields, a near field probing set-up is employed. Additionally, a digital oscilloscope is employed to measure the signal integrity (SI) performance of the PCIe channel before and after the absorber application. It is shown that an appropriate type of a microwave absorber can significantly reduce the EM radiation while maintaining the digital link SI performance. As will be presented, the measured eye diagram will be improved as a spacer is inserted between the absorber and PCB.

# Measurement details and procedures:

## Details of the tested platform and employed absorbers:

In this work, an internally developed APU/CPU reference platform provided by [5] is used since it provides the latest I/O structures to date containing USB 3.0, PCIe Gen III, SATA III and sensitive analog receivers such as GPS. Here, a PCIe channel between the main CPU and a Gen II graphic card is considered. This link is specifically targeted since the Gen II PCIe bus noise peak energy band coincides with most commonly used radio devices and it is located on the top layer of the six layer tested platform which allows easy access for near field probing and absorber application. Besides, it is expected to measure higher EM radiations from the channel as it is located at the top (outer) layer, as frequently implemented in PCB designs. During the measurements, spread spectrum clocking is master disabled through the BIOS to ensure highest radiations from the channel. To fully load the PCIe channel, standard benchmark software (Unigine Heaven) with 1920 × 1200 resolution and 60 Hz refresh rate is operated while measuring the near field radiations. The graphic card is connected to a monitor through a 2 meter cable with a DisplayPort (DP) connector.

Microwave absorbers employed in electromagnetic compatibility (EMC), EMI and RFI applications are mostly (a): magnetically loaded elastomers with spherical shaped ferrite inclusions, or (b) noise suppressors with magnetic platelets [6]. These materials mostly

operate by terminating the unwanted coupling paths or dissipating unwanted electromagnetic energy at the resonance frequencies of metallic structures [6].

Here, we have employed two wideband absorber products from [7] named BSR20 and NS1040 which are based on the spherical and platelet particles, respectively. The measured thicknesses of BSR20 and NS1040 with their adhesive backings are 0.63mm and 0.47, respectively. In addition, a 0.13mm thick paper-based spacer is also used in some tests to examine different absorber to PCB copper trace distances on the SI and EM radiation performance of the channel. BSR20 is specifically designed for cavity resonance applications as being effective from about 1-2 GHz up to 18 GHz. On the other hand, NS1040 is a noise suppressor which is highly loaded with ferrite based platelets aimed to be effective RFI instances by terminating and diverting noise leakage mechanism [7].

## Near field test set-up:

To measure the radiated electromagnetic fields from the PCIe channel, a unique magnetic loop (vertical H-field probe) and a shielded electrode surface probe (E-field probe) from [8] are employed. These probes (XF-B3-1 and XF-E09s) are usable in our desired band from 30 MHz to 6 GHz. In our experience, the correction factors of the employed probes are slightly affected by the probe angular rotations. In addition, they are almost blind to the adjacent EMI radiation sources as the probes have extremely confined resolution distance of 2mm (for the H-field probe) to 10 mm (for E-field probe) in the vertical direction. However, lab background noise as GSM signals can be picked up especially by the electric field probe. To avoid this, measurements are performed in a 10 m chamber. In each measurement, one of the probes is mounted on a positioner to accurately scan the PCB area with respect to the PCIe artwork (see Fig. 2, 3).

To increase the sensitivity of the set-up, a low noise pre-amplifier (AFS44-00102000-30-10P-44) with about 44 dB gain is inserted to feed the amplified signal into a spectrum analyzer (N9010A). During these tests, Maxhold and peak detection capabilities of the spectrum analyzer (SA) are used to report the maximum radiated fields [9]. In order to increase the repeatability of the test, the positioner is employed to hold the probe tip over the middle one of the transmitting data pairs TX0-TX7 (see Fig. 4). In this manner, the PCIe radiated fields are only picked up by the probes.

In order to examine the radiated field spectrum of the PCIe channel, a wideband measurement from 10MHz to 6 GHz is performed. As shown in Fig. 5, the embedded clock at 250 MHz and its harmonics are all present in the radiated field spectrum. As depicted in Fig. 5, the highest radiation occurs at 5 GHz which is the second harmonic of the data signal with a Nyquist frequency of 2.5 GHz and $20^{th}$ harmonic of the embedded clock. It can be noted that in this setup, the measured signal levels above -40 dBm can be of concern for EMC Class B level compliance.

Next, different resolution bandwidths (RBW) of the SA are applied in the measurement to determine the appropriate RBW which leads to highest signal to noise ratio (S/N) while offering required sensitivity. To this end, the electric and magnetic field measurements are performed as the SA center frequency is set to 750 MHz with the span 20 MHz and RBW changing from 100 KHz to 300 KHz and 1 MHz (see Fig. 6). As expected, the measured noise floor constantly increases using larger RBWs. In addition,

it appears that as RWB is set to 1 MHz enough S/N ratio can be offered by the SA. In addition, most EMC compliance measurements and RFI standard tests from 1-6 GHz are performed at 1 MHz RBW settings. In the following measurements, frequency span, RBW, and video bandwidth of SA are set to 20 MHz, 1 MHz, and 3 MHz, respectively.

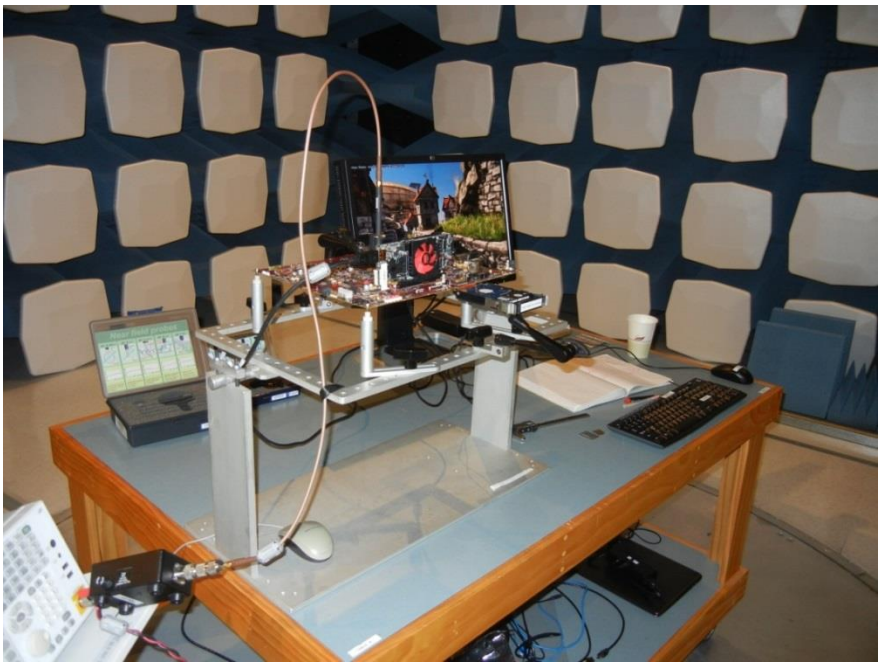


Fig. 2.: Near field measurement set-up placed in a 10 m semi-anechoic chamber.

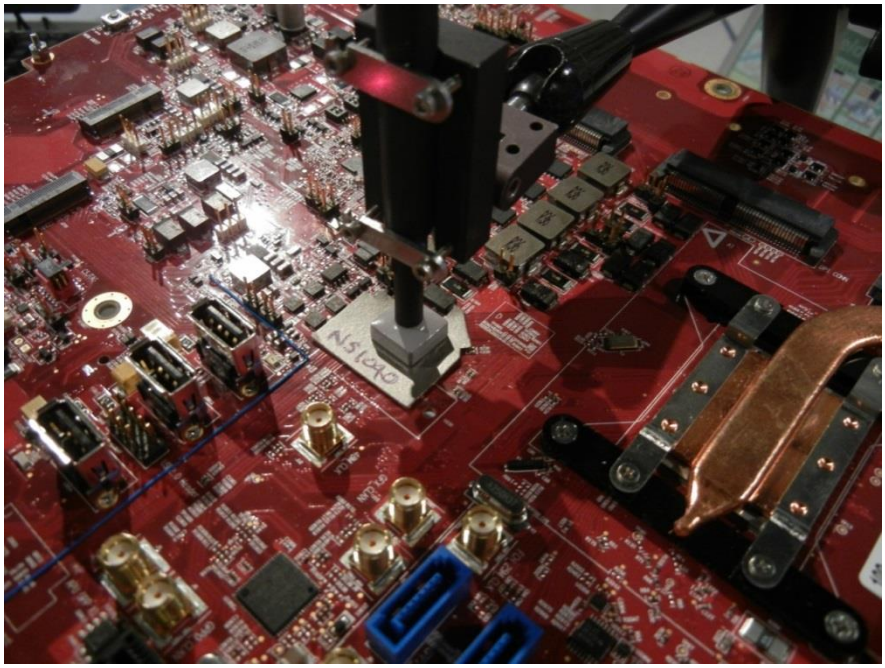


Fig. 3. Electric field probe measuring the radiated fields after the absorber is applied onto the PCIe link.

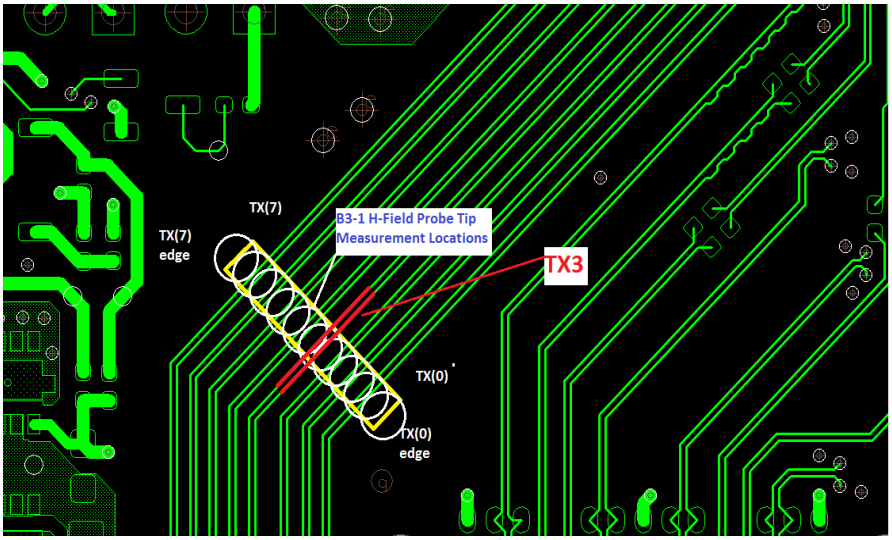


Fig. 4.: Fields are measured over the middle pair (TX3) as the probe location is fixed.

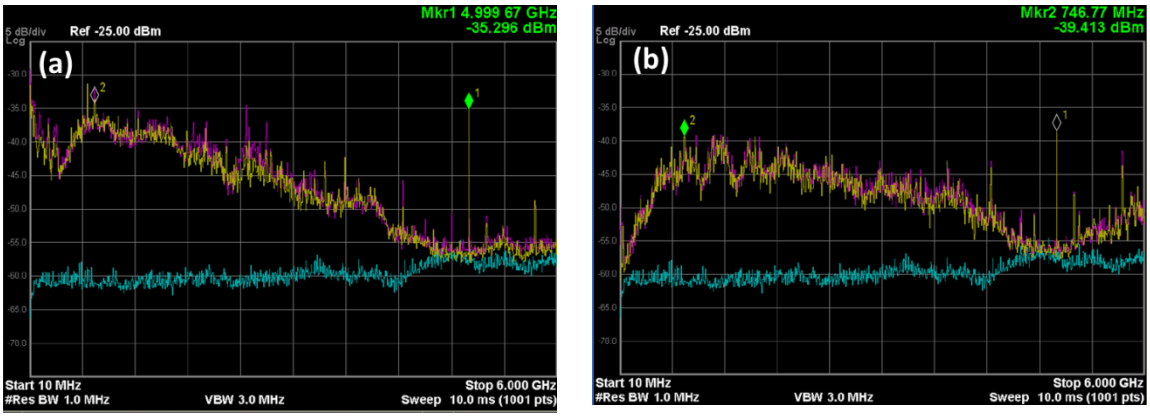


Fig. 5.: (a), (b) Measured electric and magnetic radiated fields in a wideband frequency range, respectively. In these pictures, cyan traces are the measured noise floor and yellow and purple traces are captured signals as the probe is 90° and 0° oriented compared to the PCIe bus.

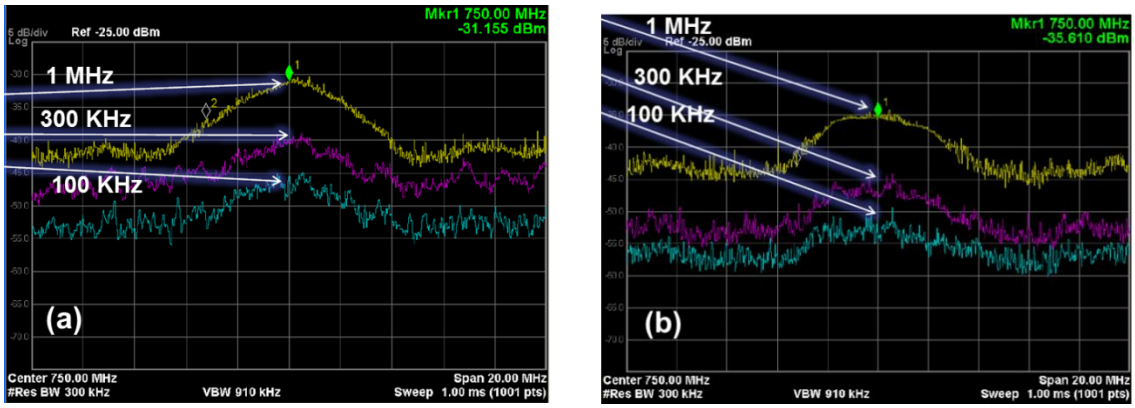


Fig. 6.: (a), (b) Measured electric and magnetic fields using the spectrum analyzer centered in 750 MHz at 20 MHz span with 1MHz, 300 KHz, and 100 KHz resolution bandwidth.

## Signal integrity measurement set-up:

To test the performance of the link and measure its signal integrity specifications before and after the absorber application, a compliance load board (CLB) is inserted into

the PCIe connector of motherboard. The middle transmit and receive pairs (TX3 and RX3) are connected to a digital oscilloscope with four channels (DSA 72004) through SMA connectors as other pairs are terminated with 50 Ω terminations (Fig. 7). Captured data is later process using standard software [10] to generate eye diagram and other interested data. In these tests, nominal data rates are 5 Gbps with unit intervals 200 ps. In addition, all equalizations are disabled during these tests.

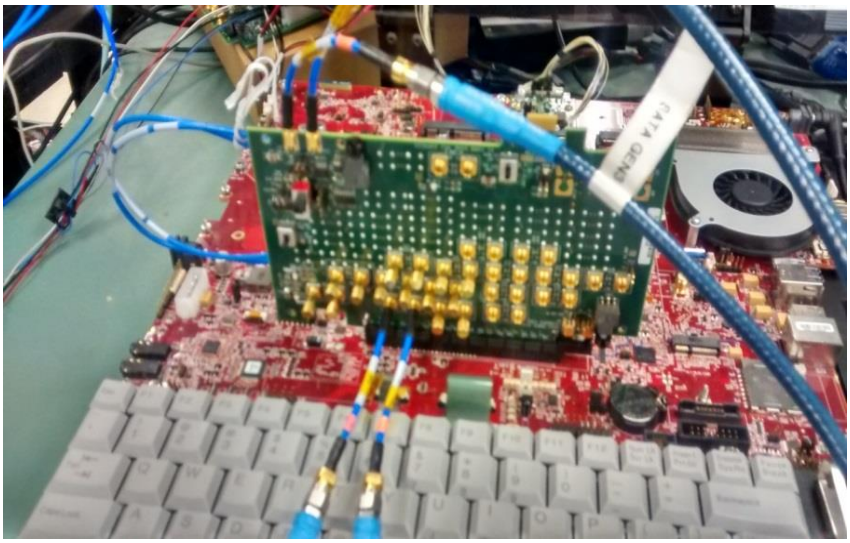


Fig. 7. A PCIe compliance load board employed for the SI performance tests.

## Results and discussion:

In this section, near field probing results and SI test performance is presented. The measurements are categorized into these cases: (1) baseline without any lossy material, (2), (3) BSR20 with and without the paper spacer, (4) and (5) NS1040 with and without the spacer.

To calculate the radiated field reductions after the absorber applications, measured electric and magnetic fields at the embedded clock harmonics are subtracted from the baseline condition case 1. In this manner, the obtained field reductions with BSR20 application with and without the spacer (case 2 and 3) are presented in Fig. 8, 9.

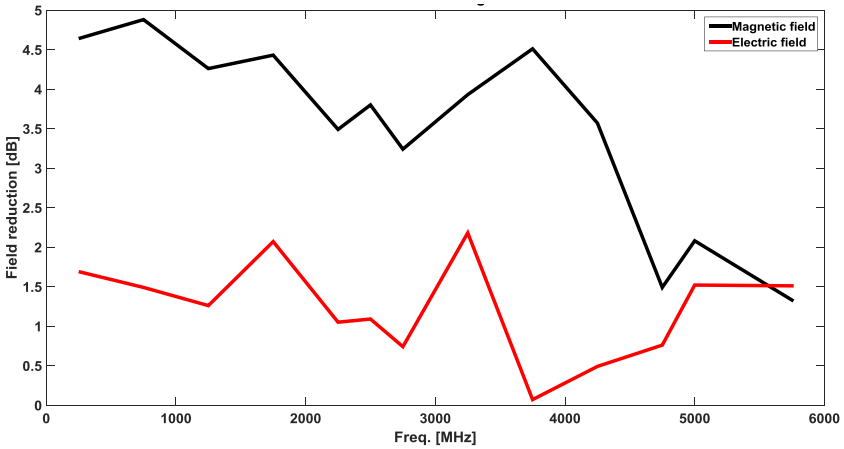



Fig. 8.: Measured electric and magnetic field reduction as a BSR20 piece with 0.13mm spacer is applied on the board.

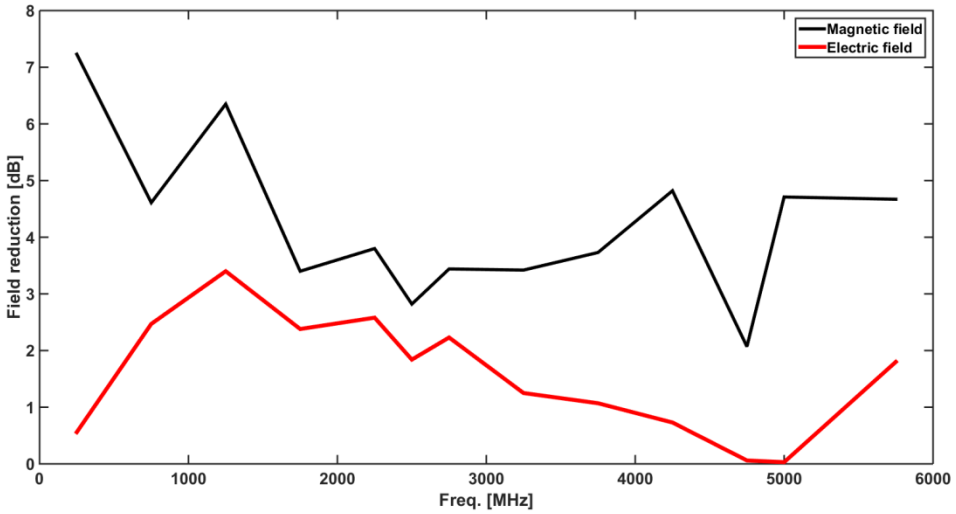


Fig. 9.: Measured electric and magnetic field reduction as a BSR20 piece is directly applied on the board

As can be seen, the field reduction obtained using the first tested absorber is not substantial especially as the spacer is inserted between the PCB and the absorber. This is expected since this type of absorber is mostly designed for cavity resonance damping solutions and doesn't necessarily offer large radiated field reduction as it is placed very close to the EM source.

In Fig. 10 and 11, radiated field reductions after placing the second absorber over a section of the PCIe channel with and without the presence of the spacer are plotted. As can be seen, this noise suppressor provides very good field reduction both in E and H field domains with and without the spacer in a broad frequency range up to 6 GHz. It is interesting to notice that the shield can offer very large electric and magnetic field dissipations even down to 750 MHz. As expected, the attachment of the spacer can slightly shrink the shield performance. However, reported field reductions are still better than 8 dB at the Nyquist frequency (2.5 GHz) and its second harmonic (5 GHz). It is interesting to notice that Wi-Fi RFI issues occur in the IEEE 802.11 b,g,n,ac bands (2.412-2.482 GHz) and 802.11 a bands (5.1-5.8 GHz). Additionally, GSM (LTE) cellular RFI issues can occur at frequencies below 800 MHz and up to 2.65 GHz.

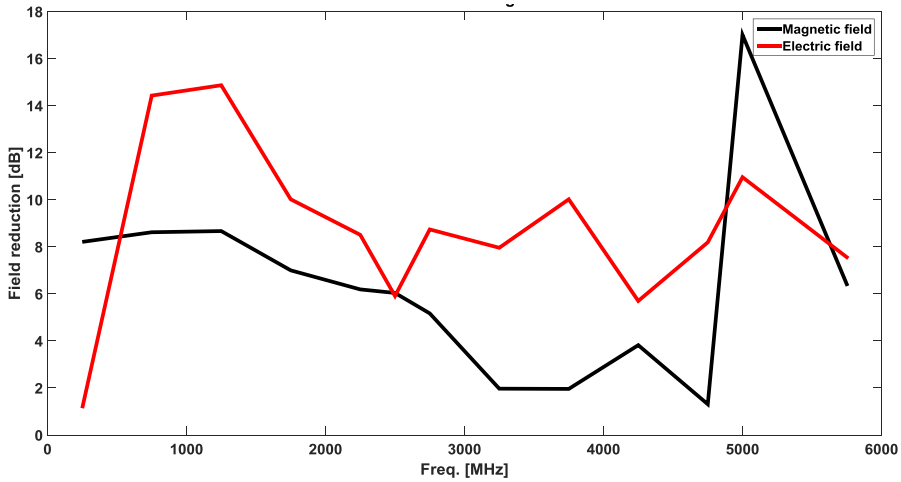


Fig. 10. Measured electric and magnetic field reduction as a NS1040 piece with 0.13mm spacer is applied on the board.

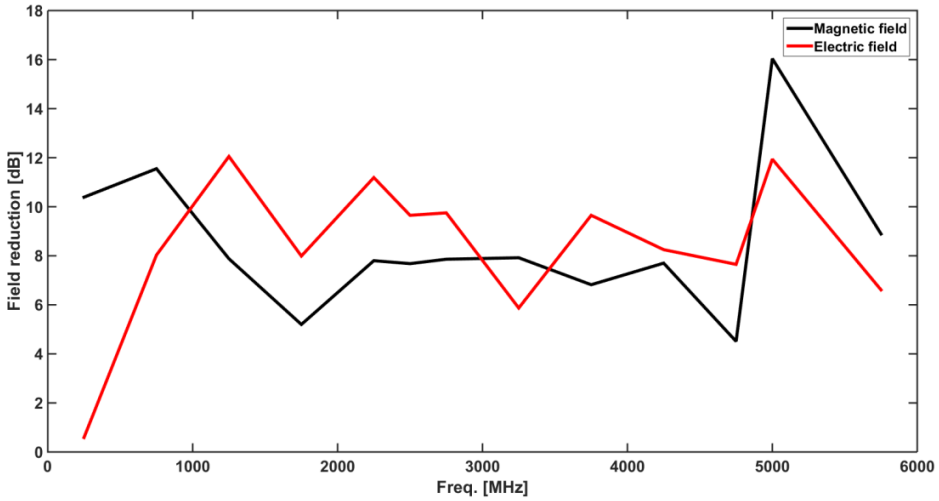


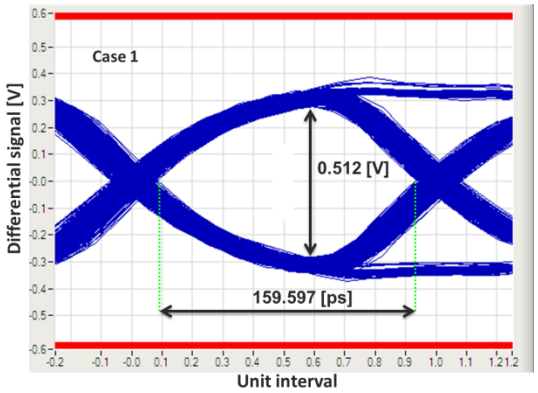

Fig. 11. Measured electric and magnetic field reduction as a NS1040 is directly applied on the board.

In Table 2, the measured eye specifications and jitter values in all the measured cases are presented. As seen, the application of the noise suppressor without the absorber (case 5) has led to about 7ps eye width and 0.0175 V eye height reductions compared to the baseline situation (case 1). This is the largest measured eye diagram degradation as the lossy material pieces are applied on the PCIe channel. Besides, it is shown that the measured total jitter at BER $10^{-12}$ has increased from 30.87 ps to 39.216 ps while the changes are reported in both random and deterministic sections. Using the compliance software, it was understood that all cases easily can pass PCIe Gen II specifications.

In Fig. 12 measured eye diagram of the five situations are presented. As shown, all measured eyes are open with considerable margins easily enabling them to pass the compliance specifications.

Table 2: Measured SI characteristics of the channel.

| Tested cases | Max Pk-Pk Jitter (ps) | Total Jitter at BER @10E-12 (ps) | Random Jitter RMS (ps) | Deterministic Jitter Delta-Delta (ps) | Minimum Eye Width (ps) | Composite Eye Height (V) |
|---|---|---|---|---|---|---|
| Case 1 | 30.870 | 40.402 | 2.265 | 8.553 | 159.580 | 0.5125 |
| Case 2 | 34.121 | 42.527 | 2.433 | 8.316 | 157.473 | 0.512 |
| Case 3 | 36.570 | 41.318 | 2.224 | 10.042 | 158.682 | 0.509 |
| Case 4 | 31.270 | 41.331 | 2.330 | 8.580 | 158.670 | 0.5103 |
| Case 5 | 39.216 | 47.403 | 2.594 | 10.919 | 152.597 | 0.495 |



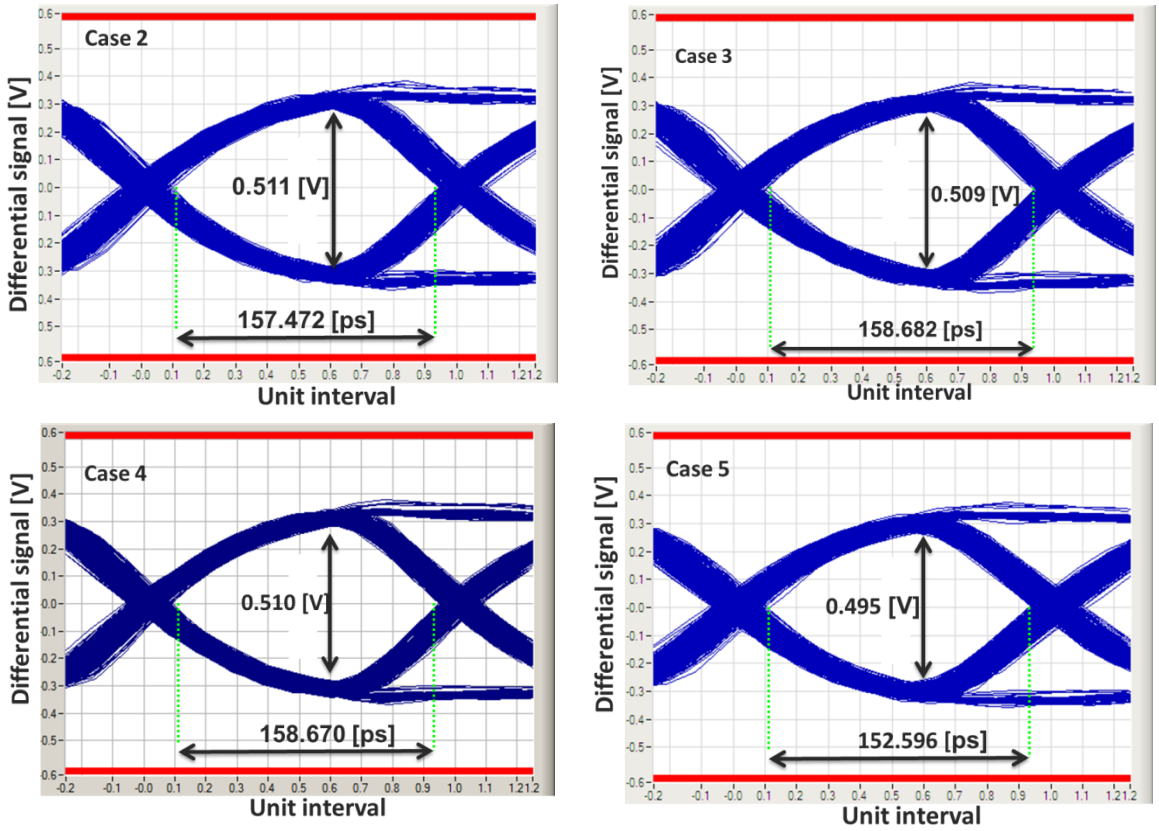



Fig. 12: Measured eye diagrams of the PCIe channel with the compliance card.

## Conclusion:

The application and placement of a microwave absorber (designed for cavity resonant damping) and a noise suppressor on a PCIe Gen II channel is examined to characterize the changes in the radiated electromagnetic field emissions and signal integrity performance of the link. It has been shown that the noise suppressor can substantially redirect and reduce the EM radiations while affecting the measured eye diagram. A sheet of paper spacer is inserted between the tested absorbers and the PCB to minimize the eye diagram reduction. It is presented that the absorber with the paper spacer can offer large field reductions without deteriorating the signal integrity performance. The absorber application is especially recommended for passing RFI internal requirements with very stringent limits in mixed signal system platforms and mobile devices.

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