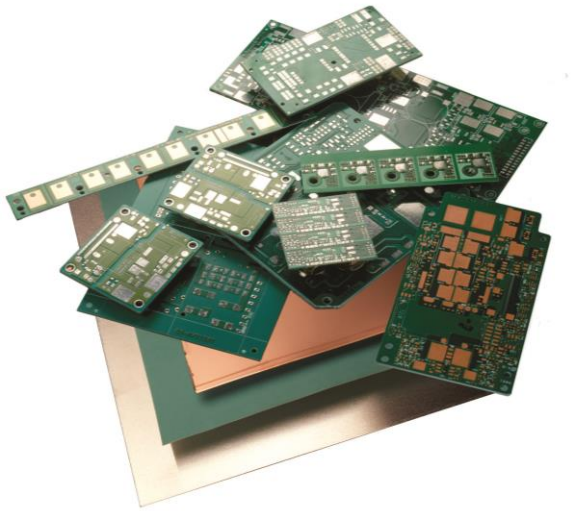
TLAM System Design Guide

PART I: PERFORMANCE AND RELIABILITY



About Laird Performance Materials

Laird Performance Materials enables high-performance electronics. We are a global company creating advanced protection solutions for electronic components and systems.

World-leading technology brands rely on us for improved protection, higher performance and reliability, custom structural designs and faster time-to-market.

We solve design issues through innovative products such as EMI suppression or absorption materials, thermal interface materials, structural and precision metals, magnetic ceramic products and multi-functional solutions. This latter product family solves multiple EMI, thermal and structural design issues simultaneously using a single process design. Industries served by Laird Performance Materials include:

- Aerospace
- Automotive electronics
- Consumer electronics
- Data infrastructure
- Defense
- Industrial
- Laptops, tablets, PCs
- Medical equipment
- Network equipment
- Telecommunications
- Test and measurement equipment
- Wearable devices

Laird™

Part I: Design Guidelines for Performance and Reliability Tlam Substrates

Tlam™ is an Insulated Metal Printed Circuit Board (Tlam SS), that can replace standard FR4 boards or ceramic substrates in power, LED, and thermal applications. Tlam type materials are also known as Insulated Metal Substrate Technology, Metal Core PCB Substrate, and Insulated Metal Substrate. The technology was developed in Japan in the late 1970s as IMST and now is used extensively in high-volume commercial and industrial products including automotive electronics, power amplifiers, power supplies, motor controllers, HV TV deflection, UPS, battery chargers, welders, LED lighting, and more.

The basic construction is a thin dielectric layer, between copper foil tracks and a metal base plate. The primary material technology is in the dielectric material, that must provide good thermal conductivity and good electrical isolation. Laird Technologies' Tlam SS dielectrics use superior thermal fillers and resins that provide exceptional thermal performance with thin dielectrics and with high thermal filler content. Tlam products are built around two basic Tlam SS dielectric systems:

1. 1KA with high thermal conductivity, unique low modulus for severe thermal cycling, and low thermal resistance applications
2. HTD with high Tg/RTI for high temperature, high-voltage, and fine-line application.

Tlam SS materials have many other secondary electrical and mechanical advantages over alternate materials.

Today, power electronic products are required to provide more performance in less space and at lower costs. As a result, the PCB or substrate must provide improved electrical, thermal, and mechanical performance. To meet these needs, designers must have the same electrical, thermal and mechanical information that would be expected with any electrical component. Laird Technologies provides this type of information in data sheets and design guidelines. The information allows designers to plan and optimize for performance, reliability, manufacturability, and cost, by using the Laird Technologies Tlam products. Tlam typically simplifies the system architecture, resulting in performance, size, reliability and cost advantages that extend beyond the substrate or board to encompass the complete assembly and end-product.

The *Tlam Part I Design Guidelines for Performance* was developed to help the user capitalize on the unique performance advantages of the Laird Technologies Tlam materials. *Part II Manufacturing Design Guidelines* contains design information for manufacturability including recommended dimensions, tolerances, materials and assembly processes, as well as suggestions for lowest cost system design. Other available application information includes fabrication guidelines, thermal multilayer applications, and more.

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List of Tlam Performance Tables

1.0 | Thermal Properties

The primary advantage of the Tlam technology is improved thermal performance while retaining good dielectric isolation at low cost. Laird Technologies Tlam uses the highest thermally conductive filler systems in this industry, which minimizes filler content and maintains the electrical and mechanical integrity of the dielectric layer. In designing with Tlam, it is important to capitalize on the thermal advantages, without adding unnecessary complexity or costs. Thermal advantages can reduce component size, track width, thermal and mechanical hardware, as well as electrical and thermal interconnects.

Thermal Conductivity of the Tlam SS 1KA and HTD Dielectric

The Tlam SS 1KA dielectric has a thermal conductivity of 3.0 W/m-K in the transverse direction.

The Tlam SS HTD dielectric has a thermal conductivity of2.2 W/m-K. The thermal conductivity of the HTD dielectric is lower than 1KA, the strength is higher, and provides the same voltage isolation at a decreased thickness. So the thermal performance of the two dielectrics is similar when the isolation values are followed.

The excellent thermal conductivity has both direct and indirect advantages for power products including the following.

- Improved heat transfer from components that improves component reliability, reduces component size and cost, eliminates component heat sinks and hardware, reduces PCB or substrate size, and increases component density and power density.
- Higher current densities in traces, vias, and connectors are possible because Tlam removes the heat and lowers the operating temperature of these conductors. Standard PCB current density rules are limited by temperature rise and using the standard PCB rules for Tlam can unnecessarily increase the size and cost of your product. Therefore, using the Tlam rules allows you to capitalize on the full advantages of Tlam.

Thermal Resistance of Tlam SS 1KA and HTD

The thermal resistance of the dielectric layer is a function of the dielectric thermal conductivity, the dielectric thickness, and the area of the power component or copper pad. The thermal resistance of the Tlam dielectric is defined as:

$R(Y) = t/\sigma A$, *where*

R(Y) = Thermal Resistance (C/W)

t = Dielectric Thickness (inch)

σ = Thermal Conductivity (W/m-K)

A = Area (square inch)

The thermal resistance per square inch (per square cm) is based on an infinite plane. In real applications, the pad and traces are small and there is an edge or heat spreading effect that reduces the thermal resistance further by transferring heat over slightly larger areas than the actual pads and traces.

The thermal resistance for a Tlam SS HTD substrate with 0.062” aluminum base plate and the Tlam HTD dielectric with 2 oz copper foil is shown in **Table 1A** for some standard power surface mount packages. The thermal resistance for substrates with Tlam SS HTD with the same packages is shown in **Table 1B**.

These are the thermal resistance for the Tlam substrate, copper foil pad through base plate. To determine the total thermal resistance junction to ambient, one must add the package resistance, Tlam substrate resistance, as well as the substrate base plate to ambient thermal resistance. Note, the heat distribution through and across the base plate can significantly reduce the thermal resistance to ambient.

TABLE 1A: Thermal Resistance Per in^2 & cm^2 vs. Tlam SS 1KA/HTD and FR4 Dielectric Thickness

Dielectric Thickness mm (mils)	Tr °C- in^2/ watt 1KA	Tr °C- in^2/ watt HTD	Tr°C- in^2/ watt FR4	Tr°C- cm^2/ watt 1KA	Tr°C- cm^2/ watt HTD	Tr°C- cm^2/ watt FR4
0.102 (4)	0.06	0.07	0.79	0.41	0.46	5.08
0.152 (6)	0.08	0.11	1.18	0.52	0.69	7.62
0.204 (8)	0.11	NA	1.58	0.70	NA	10.16

TABLE 1B: Power Packages Tr vs. Tlam SS HTD 2 oz. CU Foil and 0.062" 5052 Al Base

Dielectric Thickness mm (mils)	D-Pak °C/W	D2Pak °C/W	TO-220 °C/W	TO-247 °C/W
0.102 (4)	1.34	0.53	0.40	0.27
0.152 (6)	1.91	0.76	0.57	0.38

Thermal and Power Management

Thermal and power management must involve the total system. Key factors are maximum power, maximum junction/component temperature, maximum dielectric temperature, maximum ambient temperature, and the thermal resistance of all links between the heat source and ambient. In complex systems with multiple power sources and heat paths, Finite Element Analysis or thermal testing are the only ways to make an accurate final thermal assessment. The intent here is to list some principles, factors and relative comparisons that help the designer take the full thermal performance advantage of Tlam materials.

Tlam SS dielectrics include organic materials and, like PCBs, can be damaged by excessive heat. Laird Technologies recommends the following maximum temperatures.

In continuous or steady-state operation, the maximum power of components and traces are limited by the maximum temperature at the dielectric-to-copper foil interface, with a continuous limit of 130°C for Tlam SS 1KA08 and 150°C for Tlam SS HTD04 and HTD06.

$P(max) = \Delta T_{FB}/R(Y)_{FB}$, *where*

P(max) = Maximum Power Dissipation (watts),

$\Delta TFB = t_F - t_B$, t_F = Foil Temp.(C),

tB = Base Temp.(°C),

(Y)FB = Thermal Resistance F to B (C/watt).

The base plate temperature is a function of the total Tlam power dissipated and the thermal resistance between the base plate and ambient, which is defined as follows:

$P(Tlam) = \Delta T_{BA}/R(Y)_{BA}$, *where*

P(Tlam) = Total Power Dissipation on Tlam (watts)

$\Delta TBA = tB - tA$; tA = Ambient Temperature (C)

R(Y)BA = Thermal Resistance Base to Ambient (C/Watt)

The heat transfer from base plate to ambient will vary with application, power levels, ambient temperature, mounting, airflow, etc. The base plate can be cooled with natural forced convection or by conduction to a heat sink, bracket or other mounting surface.

The above analysis for a board with base plate and components on one side of the board, can be extended to Tlam with a copper core or a substantial inner ground and power planes that spread the heat across the board. If there is no base plate and the core copper is thin, it may be necessary to consider temperature gradients across the core or board.

TABLE 1C: Maximum Processing and Operating Temperatures of Tlam SS 1KA and HTD

Conditions	Tlam SS 1KA °C	Tlam SS HTD °C
Maximum Continuous Operation	125	150
Maximum Transient Operation	175	185
Maximum Soldering Temperature, 30 sec.	288	288
Maximum Continuous UL Rating, RTI	130 (for Tlam SS 1KA08)	150

The total thermal resistance for a component on a Tlam board or substrate is:

R(total) = Rjc + RFB + RBA, *where*

Rjc = Thermal Resistance junction to case (C/W)

While the maximum junction temperature is typically 150°C, there are several exceptions. For example, special MOSFETs for automotive temperatures have maximum Tj of 150°C to 175°C and thermally sensitive GaAs LEDs are not efficient above 100°C. It is important to determine the maximum temperature for all active and passive components in any product.

In medium power applications, the ambient air may provide sufficient heat removal from the Tlam substrate or board. The rule of thumb is $R(Y)_{BA}$ = 50°C-in^2/watt of Tlam SS surface (each side), in natural convection. The ΔT can be reduced significantly with forced convection. The $R(Y)_{BA}$ of 15-25°C-in^2/W may be more typical with guard-band, but can vary significantly with airflow, component contour, cleanliness, etc. Double-sided boards may also remove heat from the edge of the boards through wedge locks or other mechanical contacts. Any estimated ΔT_{BA} should be confirmed with Thermal Finite Element Analysis (FEA) and/or actual temperature measurements at maximum power levels.

In higher power applications or higher power modules, the heat is typically transferred by conduction to a heatsink or a metal mounting surface. The temperature of that surface may be known or can be calculated as a function of power dissipation, size, shape, ambient temperature, and air flow. These parameters are application specific and Thermagon can provide application assistance for your special products and applications.

Laird Technologies also offers a broad range of high-performance thermal interface materials that can be used between the Tlam base plate and the thermal mounting surface. These include thermal gap fillers, insulators, grease and PCM materials. Contact Laird Technologies for detailed information and literature on these products at www.lairdtech.com.

The maximum thermal resistance values provided are calculated and design guard-bands are recommended. The actual guard-band will be application specific, although a 15-25% is typical. If your application or devices are insensitive to short times above maximum rated temperatures, and transient power exceeds specified maximum continuous ratings, a 15% guard-band may not be adequate. If you have a device that is thermally sensitive or that may go into thermal runaway above the maximum rated temperature, you may need a 25% or larger guard-band.

Finally, there are thermal resistance for given areas. The actual Tlam SS dielectric thermal resistance can be improved significantly with special techniques including thicker copper, solderable heat spreaders, inner-layers, thermal vias, etc. Laird Technologies will work with you to optimize your specific products and applications.

2.0 | Dielectric Isolation

The dielectric strength or dielectric isolation voltage is a measure of the Tlam dielectric's ability to withstand high voltages between copper foil and base plate on Tlam SS substrates, as well as between foil layers or final construction of Tlam ML 1KA substrate.

Hipot Testing

The dielectric strength is verified using a hipot or hHigh potential test. This test applies a high voltage across the dielectric for a given time to ensure the dielectric does not break down. Most isolated products worldwide are tested and/or recognized per Underwriters Laboratory (UL) conditions and limits. Most other regulatory agents have equivalent or similar requirements. Important exceptions that may apply are special EC transient tests and VDE partial discharge tests.

The UL test limits and conditions can be quite complex because they are application specific. However, the majority of applications for Tlam can be covered by some select UL test and conditions for power conversion equipment. Select conditions and limits are outlined below as a measure of the dielectric strength of the Tlam SS substrates and as a guideline for typical applications. If your product must comply with any of these agencies, the applicable UL, EC, VDE, CSA or other organization should be consulted. The UL rules are conservative yet important, because of potential damage, aging, and liability issues. Therefore, they are recommended as guidelines even for products that do not require UL recognition.

All Tlam substrates or boards for finished products requiring hipot should be 100% hipot tested by the board fabricator in order to screen-out any isolation defects that were induced by the board fabrication process. It is more economical to do this screening before costly components are assembled.

Dielectric Strength and Hipot Withstand Voltages

The dielectric strength of the Tlam SS 1KA substrate is >1000V/mil and dielectric strength of the Tlam SS HTD substrate is >1500V/mil. The dielectric strength of the Tlam board or substrate must be de-rated to accommodate process and thickness variations and other manufacturing irregularities. The effective dielectric strength of the fabricated Tlam board is defined by the recommended hipot withstand voltage shown in **Table 2A**. It is recommended that all substrates/ boards be 100% tested by the fabricator for the required isolation voltage of the final product. Hipot testing above the application requirement can result in unnecessary yield loss and higher costs. Tlam layouts should include sufficient edge space to allow the hipot testing in air at the rated voltages.

The recommended Tlam SS 1KA & HTD for Vac and Vdc hipot withstand voltages are shown below in **Table 2B**.

TABLE 2A: UL Rated Dielectric Isolation Voltage Determination

Application Voltage	Rated Dielectric Isolation Voltage
<250 Vac	1000 Vac 0r 1414 Vdc
>250 Vac	1000 Vac + 2X Vac or 1.414 X (1000 Vdc + 2X Vac) Vdc
<250 Vdc	1000 Vdc
>250 Vdc	1000 Vdc + 2X Vdc

Note:
1. The rated dielectric isolation voltage must be applied for 1 minute without breakdown. Breakdown is defined as a leakage current greater than 5mA, but it may be necessary to increase this limit to compensate for a significant capacitive charging current with large area Tlam substrates.
2. The test time can be reduced to 1 second if tested at 120% of the 1-minute test voltage. However, the accelerated test requires a dielectric and spacing that will withstand 120% of the rated voltage.
3. AC hipot testing is typically done at 50-60Hz VAC.
4. DC testing must be done at 1.414 times the specified AC rated dielectric isolation voltage.
5. DC testing is usually recommended for Tlam and other insulated metal substrates because of the large charging currents associated with the thin dielectric layers.
6. The above hipot test criteria are based on UL508C for power conversion equipment requirements that are representative of other applications.

TABLE 2B: Dielectric Strength and Hipot Withstand Voltages vs. Tlam SS 1KA and HTD Dielectric Thickness

Dielectric Thickness mm (mils)	Tlam SS 1KA Vdc	Tlam SS 1KA Vac	Tlam SS HTD Vdc	Tlam SS HTD Vac
0.104 (4)	1200	750	5000	2500
0.152 (6)	2500	1500	6000	3500
0.208 (8)	3500	2500	N/A	N/A

Application/Operating Voltages

The recommended application or operating voltages are based on dielectric strength, DC life testing, partial discharge testing, and manufacturing guard-bands. There are three key operating voltages that should be considered:

1. VAC nominal or continuous
2. VDC maximum continuous
3. Vp maximum peak recurring

The recommended application voltages are shown in **Table 2C** for Tlam SS 1KA and HTD substrates.

It is important to note that these are post laminated thickness and that multilayer structures may require higher starting Tlam dielectric thicknesses to maintain these thicknesses after lamination. The final dielectric thickness will depend on layout patterns and foil area, Tlam DS copper foil thickness, and lamination process.

In general, it is important to maximize foil area with heavy copper and to add extra thickness of Tlam PP to fill the open area between heavy copper foil traces.

TABLE 2C: VAC, VDC and Vp Voltages vs. Tlam SS 1KA Dielectric Thickness

Dielectric Thickness mm (mils)	Tlam SS 1KA VAC Nom.	Tlam SS 1KA VDC MAX	Tlam SS 1KA Vp MAX	Tlam SS HTD VAC Nom.	Tlam SS HTD VDC MAX	Tlam SS HTD Vp MAX
0.102 (4)	NA	75	NA	120	225	300
0.152 (6)	120	225	300	480	950	1200
0.204 (8)	240	450	600	NA	NA	NA

Reliability and Operational Life

The Tlam PP dielectric has excellent strength and provides superior reliability to ceramic substrates and FR4 boards when used properly. The Tlam advantages arise from the inert low loss filler and the flexibility of the organic resin under thermo-mechanical expansion stresses. As with all organic materials, it is important to operate the materials under conditions where it remains stable so that all thermal, physical and electrical properties are maintained. There are four important conditions that must be examined to select the proper Tlam for reliability that are all related to the end-product application conditions. They include: temperature cycling, thermal aging, AC and DC life.

Temperature Cycling

Temperature cycling tests evaluate thermo-mechanical damage or wear-out cause by coefficient of thermal expansion (CTE) mismatch between different materials. These mismatches can occur within the substrate or between the substrate and components. The temperature cycle conditions are typically more severe than the operating conditions to accelerate failures. The delta T, cycles rate, and number of cycles may all influence the severity of temperature cycling. The CTE of components, base plate, and foil should be similar in severe application conditions. Large substrates and large components will make a given CTE mismatch more severe. Laird Technologies can provide

design guidance based on general experience or finite element analysis, but temperature cycling on actual assembled product is the only true confirmation of product life under severe temperature cycling conditions.

In general, Tlam behaves like FR4 in temperature cycling but Tlam is often used at higher power dissipation levels. Therefore, special temperature cycling requirements should be assessed. Aluminum base plates are most common, but the lower CTE of copper base plates can improve reliability in some severe conditions. The Tlam SS 1KA has a low modulus and is quite flexible. This allows absorption of significant CTE mismatch between substrate and components. This advantage can be enhanced with the thicker Tlam SS 1KA dielectric layer.

Thermal Aging

Thermal aging or wear out can occur from excessive solder time, temperature, and operation at maximum temperature for an extended time.

The Tlam SS 1KA and HTD have both been tested to the IPC T-288 solder float and delamination condition and have passed. This assures they are suitable for solder reflow at the higher Pb-Free (Sn/Ag and equivalent) solder temperatures. This also ensures that the material is suitable for the standard lower temperature Sn/Pb solder reflow conditions.

The long-term high temperature aging was performed on both Tlam SS 1KA and HTD for UL recognition. The accelerated high-temperature UL testing ensures that the Tlam SS 1KA and HTD maintain isolation and mechanical integrity to a projected 100,000 hours of continuous operation at the maximum rated operating temperature.

Based on this testing, UL has recognized the Tlam materials for the following maximum operating temperatures **(Table 2D)**.

The 1KA is a lower temperature, like the standard FR4, with a recommended maximum continuous operating temperature of 120°C to 130°C. It is generally used in lower power and lower voltage applications but can often be used at higher temperatures if the voltages are low.

The HTD contains a high temperature resin with a Tg of 170°C, with a recommended maximum continuous operating temperature of 150°C. This material is suitable for higher-power and automotive products, where both the ambient and component temperatures can be quite high. Note, in most power semiconductor components with junction temperature (Tj) at 175°C, the Tlam SS dielectric stays below 150°C because of the thermal resistance of the die and package. However, in applications with ambient temperatures near 150°C, the temperature gradient should be calculated or measured.

AC Life

The AC hipot testing only assures that there are no dielectric defects and that the dielectric does not breakdown at the required levels, which is sufficient to insure isolation in most applications. In high voltage AC applications, it is possible to have micro arcing within the dielectric that can cause dielectric breakdown over time. If such arcing exists, the wear out or aging will be accelerated with higher voltage, higher frequency, and etch through the dielectric resin, just like a standard FR4 board.

TABLE 2D: UL Electrical RTI Rating, Tlam SS 1KA & HTD vs. Dielectric Thickness

Dielectric Thickness mm (mils)	1KA Electrical RTI °C	HTD Electrical RTI °C
0.102 (4)	110	150
0.152 (6)	120	150
0.204 (8)	130	NA

This aging mechanism or wear-out can be eliminated by selecting a dielectric type and thickness that will not allow micro-arcing under the worst-case operating conditions. The micro-arcing is called partial discharge and the minimum voltage at which micro arcing begins is called the Corona Inception Level (CIL). Micro-arcing is typically defined as a discharge of greater than 5 pC per cycle, which is also the VDE criterion for CIL. There is a corresponding level, that the voltage must be reduced to for the partial discharge to stop. That voltage is called the Corona Extinction Level (CEL). The CEL is important to determine recovery from rare excursions above the CIL.

Partial discharge testing is slow and test equipment is expensive. Such testing is generally not practical as a 100% screening test. Therefore, the nominal CIL should be much higher than the peak recurring voltage, to ensure that there is never an AC wear-out mechanism present in the dielectric. The following CIL can be achieved for Tlam SS 1KA and HTD **(Table 2E)**. These are generally well above most requirements, but CIL can vary with design, layout, and process. Therefore, it should be tested and confirmed for your product in severe applications.

A good design rule of thumb is that the CIL should be three times the peak recurring voltage, but this will vary with CIL distribution.

The CIL can be confirmed with partial discharge testing during design and product qualification. If partial discharge testing is not available, it is important to do hipot testing for the full one minute of the rated maximum isolation. If a specific product has a low CIL, it has likely trapped air caused by improper lamination or layout issues with heavy copper.
Note, partial discharge begins in thin spots or air pockets in the dielectric. If the design is not sufficiently robust to guarantee no partial discharge, the thickness should be increased.

DC Life

High-voltage DC applications may add additional constraints on the selection of dielectric type and thickness. High DC voltages can produce failures in time because of ionic impurities. Wear-out may be accelerated with temperature, humidity, and high DC voltages. Therefore, it is important to choose the appropriate material and thickness for high DC voltage applications. If the Tlam is operated above the glass transition temperature (Tg), ionic contaminants can become mobile at high DC voltages. In continuous high-voltage DC applications, it is important to select a dielectric thickness that will not have DC wear-out at the maximum substrate operating temperature. The maximum recommended continuous DC operation voltages for Tlam SS 1KA @ 125C and Tlam SS HTD @ 150C are shown below in **Table 2F**.

TABLE 2E: Vp and CIL Voltage Rating vs. Tlam SS 1KA and HTD Dielectric Thickness

Dielectric Thickness mm (mils)	Tlam SS 1KA Vp Maximum Vac	Tlam SS 1KA CIL Nominal Vac	Tlam SS HTD Vp Maximum	Tlam SS HTD CIL Nominal Vac
0.102 (4)	NA	NA	300	2400
0.152 (6)	300	1500	1200	3300
0.204 (8)	600	2400	NA	NA

TABLE 2F: Maximum Vdc Rating for Tlam SS 1KA and HTD vs. Dielectric Thickness

Dielectric Thickness mm (mils)	Tlam PP Dielectric	Bias, VDC	Temperature °C	Duration Hours
0.204 (8)	1KA	1020	130	1500
0.102 (4)	HTD	1200	150	2500
0.204 (6)	HTD	1500	150	5000

DC Bias Aging

Actual accelerated life testing conditions for Tlam SS 1KA and HTD without failures are shown below **(Table 2G)**. The Tlam SS 1KA can be operated at slightly higher DC voltages if the maximum temperature does not exceed the Tg of 105°C. However, no HV DC Life testing has been performed at 105°C to determine the actual limits because accelerated temperatures change the failure mechanisms. The Tlam SS HTD can, in principle, be operated up to the Tg of 170°C with similar expected DC life results. However, no testing has been performed above 150°C to confirm the dielectric integrity with HV DC bias.

TABLE 2G: Accelerated Bias Aging for Tlam 1KA and HTD vs. Dielectric Thickness

Dielectric Thickness mm (mils)	Tlam SS 1KA @ 130°C MAX Vdc	Tlam SS HTD @ 150°C MAX Vdc
0.102 (4)	106	450
0.152 (6)	225	950
0.204 (8)	950	NA

3.0 | Copper Foil Resistivity

The copper foil used for Tlam is identical to foil used on standard FR4 PCB (although generally thicker) because Tlam is typically used for higher power products. The better thermal properties of the Tlam keep the tracks cooler, which reduces the resistivity for a given current level. The bulk resistivity of copper is 0.67 µohm @ 20°C and 0.96 µohm @ 130°C.

The sheet resistivity for 1 oz through 4 oz copper are given in Table 3.1 at 20°C and 130°C, while the sheet resistivity of selected copper foil weights are shown below at 20°C and 130°C. The relationship between sheet resistivity and track resistance is given below as a function of line length, width, and thickness.

R = rL/W, *where*

R = Resistance (milli-ohms)

r = Sheet Resistivity (milli-ohms/square)

L = Length of Track (inch)

W = Width of Track (inch)

TABLE 3A: Copper Foil Sheet Resistivity vs. Foil Weight

Copper Foil Weight, oz	Resistivity @ 20°C milli-ohms/in^2	Resistivity @ 130°C milli-ohms/in^2
1	0.48	0.69
2	0.24	0.34
3	0.16	0.23
4	0.12	0.17

4.0 | Maximum Copper Foil Current with Tlam SS 1KA and HTD

The maximum trace current carrying capability for Tlam is significantly higher than that of standard FR4 printed circuit boards. The primary reason is that the higher thermally conductive Tlam PP dielectric takes the heat away; the secondary effect is the lower resistivity at the lower operating temperature based on the TCR of copper.

The maximum current vs. line width has been model based on a ΔT of 50°C, and are shown for 1 oz, 2 oz, 3 oz, and 4 oz copper. The maximum currents are shown in **Table 4A**.

Maximum foil temperature of Tlam SS 1KA is 90°C, 100°C, and 110°C for 0.102, 0.152, and 0.204 mm dielectric thickness respectively. The Tlam SS HTD has a 130 °C maximum foil rating for 0.102 and 0.152 mm dielectrics. The maximum current for foil on HTD could be higher because the maximum temperature could be increased to 150°C.

Maximum current (A) for Tlam SS 1KA and HTD with design guard-bands are shown below for select dielectric thicknesses.

TABLE 4A: Maximum Steady-State Current vs. Line Width of Tlam SS 1KA & HTD SS

Foil Weight (oz.)	Line Width mm (mils)	Tlam 1KA06 MAX A	Tlam 1KA08 MAX A	Tlam SS HTD04 MAX A	Tlam SS HTD 06 MAX A
1	0.254 (10)	8	7	8	6
1	0.518 (20)	15	13	16	11
1	1.270 (50)	38	33	40	29
1	2.540 (100)	77	67	81	57
1	6.350 (250)	192	166	202	143
2	0.254 (10)	11	9	11	9
2	0.518 (20)	22	19	23	14
2	1.270 (50)	54	47	57	47
2	2.540 (100)	109	94	114	93
2	6.350 (250)	272	235	286	233
3	0.254 (10)	13	12	14	11
3	0.518 (20)	27	23	28	23
3	1.270 (50)	67	58	70	57
3	2.540 (100)	133	115	140	114
3	6.350 (250)	333	288	350	286
4	0.254 (10)	15	13	16	13
4	0.518 (20)	31	26	32	28
4	1.270 (50)	77	67	81	57
4	2.540 (100)	154	119	162	114
4	6.350 (250)	384	298	404	287

Notes: 1. These are recommended design currents that are guard-banded at 80% of the calculated maximum currents. The guard-bands are intended to compensate for tolerances in dimensions and material properties.

5.0 | Capacitance with Tlam SS 1KA and HTD

The Tlam SS dielectric has a unique filler system with a lower dielectric constant and lower dielectric loss, relative to competitive thermal materials.

The Tlam SS 1KA offers an exceptionally low dielectric constant for thermal dielectrics where the dielectric constant is 4.3 @ 1KHz and 3.9 @ 1 MHz. The lower capacitance reduces capacitive coupling, as well as associated noise, cross talk, and ground current.

These advantages may be even more important at higher frequencies and higher voltages. They can contribute greatly to overall switching efficiency. The associated low dielectric loss is also important in many applications.

The Tlam SS HTD offers a similar dielectric constant to conventional thermal materials, which is sometimes important as an interchangeable second source. The dielectric constant is 5.1 @ 1KHz and 4.8 @ 1MHz – slightly lower than most thermal dielectrics – allowing for thinner layers with lower thermal resistance.

C = 0.225KA/t, where

C = Capacitance (pF)

K = Dielectric Constant

A = Pad Area (square inches)

t = Dielectric Thickness (inch)

The capacitance per area is based on an infinite plane. When it is important to calculate the actual capacitance value, use the actual area plus an additional edge effect for more precise values. The edge effect can be better simulated by adding 1.2 times the dielectric thickness to the perimeter of the pad or track.

TABLE 5A: Capacitance vs. Tlam SS 1KA and HTD Dielectric Thickness

Dielectric Thickness mm (mils)	Capacitance Tlam SS 1KA @ 1KHz pF/in^2	Capacitance Tlam SS 1KA @ 1MHz pF/in^2	Capacitance Tlam SS 1KA @ 1KHz pF/in^2	Capacitance Tlam SS 1KA @ 1MHz pF/in^2
0.102 (4)	244	230	287	270
0.152 (6)	162	153	191	180
0.204 (8)	122	115	NA	NA

6.0 | Low Inductance Tlam Traces

The Tlam SS 1KA and HTD offer an extremely low track inductance, relative to wires, standard PCB tracks, ceramic substrate tracks, connectors, and terminals.

The thin dielectric layer between the tracks and the base plate provides inductance reduction, similar to a laminated bus bar with an equal current in the opposite direction. This allows devices to be switched at higher di/dt with lower peak switching voltages and with lower switching losses. The lower switching voltage peaks may allow the use of lower voltage switching devices that can inherently reduce device cost. Often the lower voltage devices have lower conduction losses.

The precise inductance calculation can be quite complex for specific layout geometries, but it is possible to make good estimates under special conditions.

Because inductance is important to applications at high frequencies or high di/dt, it is possible to consider only the external inductance or to consider that L = L(ext) at high frequencies greater than 1 Mhz or at high di/dt greater than 1000A/uS.

L = L(ext) = 32.0 t L/W, *where*

L = Inductance at f > 1 MHz (nH)

L(ext) = External Inductance (nH)

T = Dielectric Thickness (inches)

L = Track Length (inches)

W = Track width (inches)

Since low inductance is most important at high frequencies or high di/dt, this equation is sufficient for estimating maximum noise or peak voltages in such applications. A very rough rule of thumb for the inductance at 1 KHz is 3.6 times the L(ext). **Table 6.1** shows the inductance per linear inch vs. line width, for Tlam traces at 1 MHz with 0.102 to 0.204 mm dielectric thickness and 0.25 to 6.35 mm line width.

The following table provides the Tlam trace Inductance @ 1 MHz for some selected dielectric thicknesses and line widths.

This is effective inductance at high frequency or high di/dt. It will allow the calculation of voltage spikes resulting from high di/dt. Note, the values are the same for 1KA and HTD Tlam.

ΔV = L di/dt, *where*

ΔV = Induced Voltage Spike (volts)

L = Effective Inductance @ high frequency (H)

di/dt = Rate of Current Change (A/sec)

For example, if you switch a device at a di/dt = 1500A/uS, and you have a stray inductance of 5 nH, the resulting voltage spike will be 7.5 volts. In most products or associated devices, terminals and connectors make a much larger contribution to the stray inductance than long Tlam traces.

TABLE 6A: Inductance vs. Tlam SS 1KA & HTD Dielectric Thickness and Line Width

Dielectric Thickness mm (mils)	Line Width 0.25 mm (10 mils)	Line Width 0.63 mm (25 mils)	Line Width 1.27 mm (50 mils)	Line Width 2.54 mm (100 mils)	Line Width 6.35 mm (250 mils)
0.102 (4)	12.8	5.1	2.6	1.3	0.5
0.152 (6)	19.2	7.7	3.8	1.9	0.8
0.204 (8)	25.6	10.2	5.1	2.6	1.0

7.0 | Electrical Vias Between Foil Layers

As with standard PCBs, copper plated vias are used to make electrical connections through the Tlam DS dielectric layer, connecting traces on different foil layers. In a standard PCB, the FR4 acts as a thermal insulator where the via current ratings are limited by the FR4 thermal conductivity and associated allowable temperature rise.

Maximum Via Current with Tlam DS 1KA

The Tlam DS 1KA vias have a much higher current rating because the Tlam DS 1KA dielectric provides excellent thermal conduction of the heat from the vias and because the metal base plate or core distributes and removes the heat generated by the vias.

The maximum via currents have been calculated for a Tlam DS 1KA with two layers of copper foil and two Tlam ML dielectric layers, all on an aluminum base plate. The vias are between the two copper foil layers. The maximum base plate temperature has been set at 80°C and the current has been calculated as required to rise the via to a temperature of 130°C for 1KA. **Table 7A** shows the maximum via current vs. dielectric thickness with 0.33, 0.53 and 0.76 mm diameter vias, with 1.27 mm and 2.54 mm via pitch or center-to-center via spacing.

The Maximum Via Currents are listed below in **Table 7A**.

The maximum currents shown are calculated based on the maximum rated temperatures. The actual designs should be guard-banded to accommodate material, process and design variations, as well as tolerances.

As with other parameters, the necessary guard-band will vary by product and application, but it is typical to design for 75% of the calculated maximum current.

TABLE 7A: Maximum Via Current vs. Tlam ML 1KA Dielectric Thickness

Via Diameter mm (mils)	Lower Tlam 1KA Thickness mm (mils)	Upper Tlam 1KA Thickness mm (mils)	MAX Via Current A 0.025 mm	MAX Via Current A 0.051 mm	MAX Via Current A 0.025 mm	MAX Via Current A 0.051 mm
0.33 (13)	0.152 (6)	0.152 (6)	83	118	62	88
0.33 (13)	0.204 (8)	0.204 (8)	63	89	47	67
0.53 (21)	0.152 (6)	0.152 (6)	107	153	80	114
0.53 (21)	0.204 (8)	0.204 (8)	80	116	60	87
0.76 (30)	0.152 (6)	0.152 (6)	120	174	90	130
0.76 (30)	0.204 (8)	0.204 (8)	90	131	68	98

Electrical and Thermal Via Model

The vias can greatly enhance the heat transfer through the dielectric layer where isolation is not required. The maximum via thermal resistances are calculated with hexagonal pad of copper foil in both foil layers. The pads and vias form a thermal cell with an area of 0.864 times the via pitch. The maximum via currents apply to an individual cell or the vias in an array of cells. The vias also enhance the thermal conductivity from a pad on the upper foil to the base plate. The thermal resistances of the thermal via pads are presented in section 8.0.

Maximum Via Resistance with 1KA

The via may be the thinnest copper interconnect in the Tlam substrate or board. That copper can have a maximum current with a temperature as high as 130°C for 1KA. At 130°C the resistivity of copper is 0.37 µohm-cm the via resistance for Tlam DS 1KA has been calculated based on a temperature of 130°C. The maximum via resistance vs. dielectric thickness is shown in **Table 7B** for various via sizes and plating thicknesses. The via resistance at nominal currents will be less than at maximum current. It can be calculated based on the TCR of the copper and the actual via temperature. Single via resistances with 50 mil pitch ΔT=50C and 2 oz Cu foils with 0.025 mm Cu plating are shown below with 0.33, 0.53 and 0.76 mm vias, and 0.152 and 0.204 mm dielectric thicknesses.

These via resistances are guidelines and your layout or application may vary. Therefore, it is recommended that the maximum via resistances be confirmed with FEA and/or measurement on the actual design and board fabrication process. Plating tolerances for the vias are hard to control. If the design is marginal, it may be better to increase the nominal plating thickness to accommodate the tolerances.

TABLE 7B: Via Resistance versus Tlam ML1KA Dielectric Thickness, at Maximum Current

Via Diameter mm (mils)	Lower Dielectric Thickness mm (mils)	Upper Dielectric Thickness mm (mils)	Via Resistance @ 20°C micro ohms	Via Resistance @ 130°C micro ohms
0.33 (13)	0.152 (6)	0.152 (6)	105	150
0.33 (13)	0.204 (8)	0.204 (8)	140	200
0.53 (21)	0.152 (6)	0.152 (6)	63	990
0.53 (21)	0.204 (8)	0.204 (8)	84	120
0.76 (30)	0.152 (6)	0.152 (6)	43	62
0.76 (30)	0.204 (8)	0.204 (8)	58	130

8.0 | Thermal Via Applications

Multiple vias between copper foil layers can significantly enhance thermal conductivity between those layers.

Thermal vias can be much more effective in Tlam than in standard PCBs, because Tlam provides a means to transfer the heat from the lower layer to a heatsink, bracket or ambient. The improved thermal dissipation not only cools the vias and tracks, but also significantly reduces the thermal resistance for power devices soldered to the upper foil pads. The technique is useful in removing heat from both packaged devices and chips, and is especially effective in complex, multi-layer board applications, such as single board computers and motor drive boards. Thicker copper foil or soldered copper heat spreaders can greatly increase the effective area of heat transfer.

Thermal Resistance of Tlam Multi-layers with Thermal Vias

The thermal resistance per square Inch from upper foil to base plate vs. dielectric thickness is given in **Table 8A** for Tlam DS 1KA. The graphs provide thermal conductivity for ΔT=50°C with a maximum base plate temperature of 80°C for 0.33, 0.53, and 0.76 mm vias, and for 1.27 and 2.54 mm pitch. The Tlam PP thicknesses shown are per layer.

As with the electrical vias, these thermal resistance values between upper foil and base plate are based on a hexagonal cell of metal in both foil layers. Extending the inner foil layer or increasing copper thickness can reduce the thermal resistance further. Typically, these reductions will be small but, in some layouts and applications, they can offer significant improvements.

The thermal resistance per square inch is shown below for selected 1KA dielectric thicknesses, select via size, ΔT=50°C, T(base)=80°C, 2 oz Cu foil with 0.025 and 0.052 mm Cu plating, and a 1.27 and 2.54 mm via pitch.

General Thermal Via Considerations

As with the electrical via, a design guard-band is recommended to accommodate process, material, as well as layout variations and tolerances. Typically, a 20% guard-band will be sufficient, but this may vary with product and application. Therefore, the necessary guard-band should be determined by FEA and/or testing for critical applications.

Thinner dielectric layers can best reduce the thermal resistance while a thinner lower dielectric layer provides the best improvement to thermal via configurations.

TABLE 8A: Multilayer with Thermal Vias between Upper Layers; Thermal Resistance vs. Tlam ML 1KA Dielectric Thickness

Via Diameter mm (mils)	Lower Dielectric Thickness, mm (mils)	Upper Dielectric Thickness mm (mils)	1.27 mm Via Pitch 0.025 mm Cu °C/watt	1.27 mm Via Pitch 0.052 mm Cu °C/watt	2.57 mm Via Pitch 0.025 mm Cu °C/watt	2.57 mm Via Pitch 0.052 mm Cu °C/watt
0.33 (13)	0.152 (6)	0.152 (6)	0.105	0.095	0.156	0.128
0.33 (13)	0.204 (8)	0.204 (8)	0.137	0.125	0.199	0.164
0.53 (21)	0.152 (6)	0.152 (6)	0.106	0.970	0.138	0.117
0.53 (21)	0.204 (8)	0.204 (8)	0.140	0.128	0.177	0.151
0.76 (30)	0.152 (6)	0.152 (6)	0.121	0.111	0.130	0.113
0.76 (30)	0.204 (8)	0.204 (8)	0.160	0.147	0.167	0.146

More small vias typically reduce the thermal resistance, but add cost; thicker copper also reduces thermal resistance, but at increased costs for both materials and manufacturability. For example, Tlam PP 1KA06 dielectrics with 0.33 mm vias, 1.27 mm pitch, and 50°C ΔT, has a thermal resistance per square inch, 0.083 C/W with 1 oz copper and 0.25 mm Cu plating, 0.077 C/W with 2 oz copper, and 0.035 mm Cu plating.

Thermal Vias in Applications without Base Plates

Thermal vias provide significant thermal improvement in products without a base plate. Copper foils can be used as thermal planes to distribute heat over the entire available board surface and heat can be transferred to the thermal planes through vias and/or isolated adjacent pads. Heat dissipation can be optimized by uniformly distributing the heat across the board, which can be done with component placement and thicker thermal copper planes. Once the board is at a relatively uniform temperature, more copper will only add cost. Also when the board is at a common temperature, the thermal resistance from board to ambient can be more easily estimated and calculated. The inner copper core can be quite effective with high-density double-sided boards. The thermal performance of the inner copper core boards is further enhanced with wedge-locks and other thermal-mechanical edge heatsinking. Thermal vias can also be used at the edge of the boards to transfer heat from the planes to the wedge locks or other thermal-mechanical edge contacts.

These techniques are useful when heat sinks are not used and enhanced with forced air or thermal mounting brackets to the thermal plane. The Tlam PP dielectric is relatively soft and flexible. It may require additional support when not used with a base plate. This often includes a thin layer of FR4 in the lamination and may be required for large boards, heavy components or for boards that serve a structural function. The FR4 may also be required in an unbalanced layout that would warp from thermo-mechanical stresses. The thickness and location of support board layers should be chosen so as not to limit the thermal performance of the Tlam system.

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TLAM-GUIDE-PART-1_OCT2020