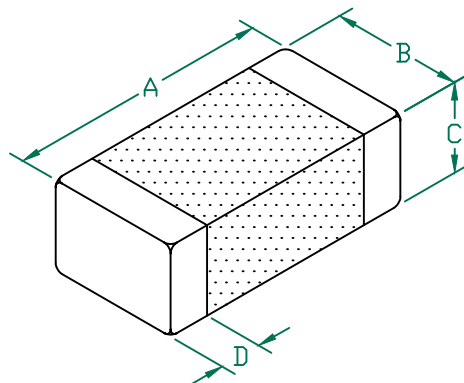


HI1206N101R-10

PHYSICAL DIMENSIONS:

A	3.20 [.126]	+ 0.20 [.008]
B	1.60 [.063]	+ 0.20 [.008]
C	1.10 [.043]	+ 0.20 [.008]
D	0.51 [.020]	+ 0.25 [.010]



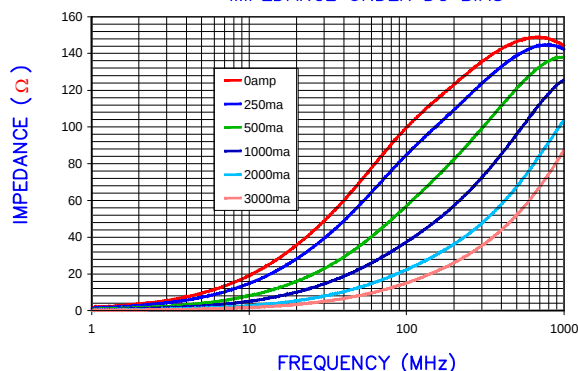
ELECTRICAL CHARACTERISTICS:

Z @ 100MHz (Ω)	DCR (Ω)	Rated Current
Nominal	100	
Minimum	75	
Maximum	125	0.035 3000 mA

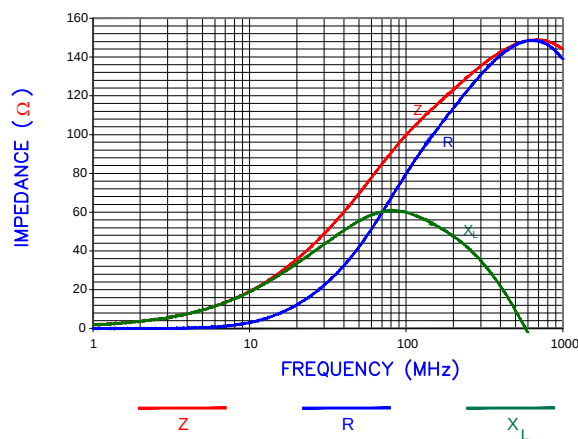
NOTES: UNLESS OTHERWISE SPECIFIED

1. TAPED AND REELED per CURRENT EIA SPECIFICATIONS 7" REELS, 3,000 PCS/REEL, EMBOSSED PLASTIC TAPE.
2. TERMINATION FINISH IS 100% TIN.
3. COMPONENTS SHOULD BE ADEQUATELY PREHEATED BEFORE SOLDERING.
4. OPERATEING TEMPERATURE TEMP: $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$ (INCLUDING SELF-HEATING)

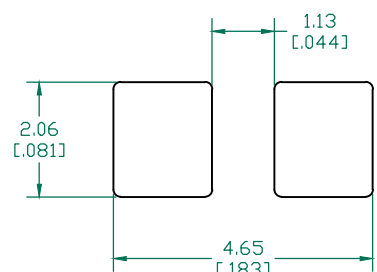
Z vs FREQUENCY
IMPEDANCE UNDER DC BIAS



|Z|, R, AND X vs. FREQUENCY

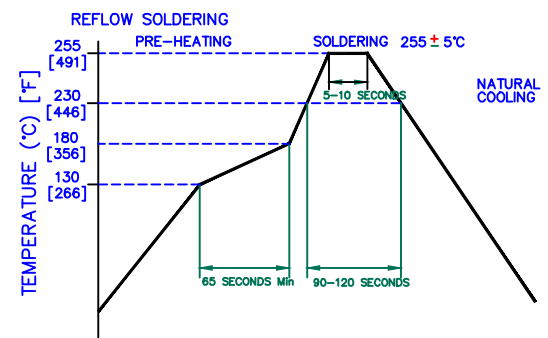


LAND PATTERNS FOR REFLOW SOLDERING



(For wave soldering, add 0.762 [.030] to this dimension)

RECOMMENDED SOLDERING CONDITIONS



AGILENT E4991A RF Impedance/Material Analyzer
HP 16194A Test Fixture. TEST REF. 3124



DIMENSIONS ARE IN mm [INCHES].				This print is the property of Laird Tech. and is loaned in confidence subject to return upon request and with the understanding that no copies shall be made without the written consent of Laird Tech. All rights to design or invention are reserved.			
F	OPERATING TEMPERATURE UPDATE LAIRD LOGO AND REFLOW CURVE	08/05/13	QU				
E	UPDATE COMPANY LOGO	06/15/09	JRK				
D	ADD ROHS SYMBOL MODIFY NOTE 2	01/19/07	JRK	PROJECT/PART NUMBER: HI1206N101R-10			
C	ADD DC BIAS CURVE COR. LANDPATTERN	03/07/03	JRK				
B	REMOVE NOTE 3	09/14/01	JRK	DATE:	01/12/01	SCALE:	NTS
A	ORIGINAL DRAFT	01/12/01	BAC	CAD #	HI1206N101R-10-F	TOOL #	-
REV	DESCRIPTION	DATE	INT	SHEET: 1 of 1			